REMARKS

The Office Action dated December 17, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 3, 7 and 8 have been amended, and claims 5 and 6 have been cancelled without prejudice. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-4 and 7-9 are pending in the present application and are respectfully submitted for consideration.

Claims 8 and 9 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In making the rejection, the Examiner took the position that the phrase "information about whether ECC correction is possible" makes claims 8 and 9 omnibus claims. Applicant respectfully traverses the rejection, and requests for reconsideration.

The above phrase at issue does not render claims 8 and 9 omnibus claims because it clearly points out the subject matter being claimed. Specifically, the phrase clearly recites the subject matter regarding information that can indicate if the function of ECC correction can be accomplish. In other words, the information is an indicator of whether the ECC correction can be performed. Accordingly, Applicant submits that claims 8 and 9 are fully in compliance with U.S. patent practice, and requests the withdrawal of the rejection.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi (U.S. Patent No. 6,058,047, "Kikuchi") in view of Ma et al. (U.S. Patent No.

5,956,473, "Ma"). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi. Applicant respectfully submits that each of claims 1 and 4 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a method of marking an initial defective block in a semiconductor memory device having a memory area thereof divided into a plurality of blocks and provided with an ECC function. The method includes the steps of detecting an initial defective block, and writing an ECC code causing an ECC error in a predetermined area of the initial defective block.

Claim 4 recites a method of searching for an initial defective block in a semiconductor memory device having a memory area thereof divided into a plurality of blocks and provided with an ECC function. The method includes the steps of reading data from a predetermined area of a given block, performing an ECC check on the read data, and identifying the given block as a defective block if an ECC error is detected.

Accordingly, at least one of the essential features of the present invention with respect to claim 1 is the step of "writing an ECC code causing an ECC error in a predetermined area of the initial defective block," and with respect to claim 4 is the step of "identifying the given block as a defective block if an ECC error is detected." As such, the present invention results in the advantage of efficient control of defective blocks within a semiconductor memory device.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claims 1 and 4, and therefore fails to provide the advantages that are provided by the present application.

Kikuchi discloses a flash memory 2 divided into a plurality of blocks 3, and includes a main controller, that is, a main memory area 31 including a good block to which a logical address managed by the host computer, is assigned, and a backup memory area 33 including backup blocks 32 each used as a substitution for a good block of the main memory area 31. Each block 3 of Kikuchi has a data region 4 in which data can be written and a redundant region 5 in which the management information of the block is written. The redundant region 5 further includes a first region 51 in which an ECC corresponding to the data written in the data region 4, can be written, a second region 52 serving as a count storage region for storing the count value corresponding to the number of 1-bit errors detected when data written in the block 3 are read, and a third region 53 for storing identification information as to whether the block 3 is good or no-good.

Ma discloses a flash memory system 100 containing one or more flash memory chips for storing data and program, such as chips 102-104. Each memory chip may be divided into several memory blocks. Each memory block contains a large number of erasable programmable read-only memory cells that can store bits of data. Ma also discloses that chip 102 is divided into blocks 112a-123b. Similarly, chips 103 and 104 are divided into blocks 112b-123b and 112c-123c, respectively. Each of chips 102-104 is divided into the same number of blocks.

Applicant respectfully submits that each and every element recited within claims 1 and 4 is neither disclosed nor suggested by Kikuchi and/or Ma, taken alone or in combination. In particular, Applicants submit that the method of marking an initial

defective block and the method of searching for an initial defective block in a semiconductor memory device, as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the step of "writing an ECC code causing an ECC error in a predetermined area of the initial defective block," with respect to claim 1; and the step of "identifying the given block as a defective block if an ECC error is detected" with respect to claim 4.

It is submitted that Kikuchi merely teaches erasing the flag "1" of the quality identification information in response to an uncorrectable error detected by an ECC error check, thereby permanently prohibiting the further use of the block as a defective block. Kikuchi further shows that even if the error is correctable, the flag "1" of the quality identification information is still erased if the error count has reached a predetermined number, thereby permanently prohibiting the further use of the block. (See column 4, lines 27-57 of Kikuchi.)

Accordingly, Kikuchi merely teaches the marking of a defective block by writing/erasing the flag value of the quality identification information that is separate from an ECC code. In addition, Kikuchi neither teaches or suggests marking a defective block by writing an ECC code causing an ECC error.

Ma merely teaches a method of managing a flash memory by skipping over defective cells while the good cells are used to store data, and does not teach or suggest marking a defective block by writing an ECC code causing an ECC error of the present invention.

In view of the above, Applicant submits that neither Kikuchi nor Ma, taken alone or in combination, teaches or suggests each and every element recited in claims 1 and 4 of the present application, and therefore are allowable.

Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of Ma and further in view of Cooper (U.S. Patent No. 6,397,357).

As claims 2 and 3 depend from claim 1, Applicant submits that each of these claims incorporates the patentable aspects therein, and is therefore allowable for at least the reasons as set forth above with respect to the independent claims.

Claims 5-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kishino (U.S. Patent No. 6,526,537, "Kishino") in view of Cooper. Claims 5 and 6 have canceled without prejudice, and therefore the rejection with respect to these claims are now moot. As for claims 7-9, Applicant respectfully submits that each of claims 7-9 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 7 recites a semiconductor memory device having a memory area divided into a plurality of blocks, an ECC generation circuit that generates an ECC code for data written into and for data read from an accessed block, and an ECC suspension circuit that suspends an ECC generation function of said ECC generation circuit so as to allow the ECC code to be directly written into said memory area from an exterior of the semiconductor memory device. Information about the presence or the absence of an ECC error is output to the exterior of the semiconductor memory device in response to a predetermined command input after a data read operation.

Kishino discloses a storage capable of reducing, in the correction/detection of errors of data with an ECC, the ratio of check bits to data bits and thereby reducing the required number of memory devices as far as possible white remedying the fault of a single memory whose number of bits is increasing. In addition, Kishino discloses a storage capable of generating an ECC for data and adding the ECC to the data to thereby form a read/write unit, an ECC is generated for each N of the data, equally divided into N ECC code parts and then respectively added to the N data to thereby constitute read/write units. The read/write units are continuously written and read out of N continuous addresses of a memory device.

Cooper discloses a system and method for testing the error detection and correction ("ECC") capabilities of an ECC memory controller. The system of Cooper uses the natural state of the bus to induce one- or two-bit memory errors by disabling the ECC capabilities of the controller and then writing a test data pattern that is one or two bits different than a data pattern that would result in an ECC code equal to the natural state of the bus and an ECC code equal to the natural state of the bus to a selected memory location. At that point, the ECC capabilities of the memory controller are reenabled and the memory location to which the test data pattern was previously written is read and its ECC code generated.

Applicant submits that Kishino only teaches an ECC generation circuit that generates an ECC code for read/write data. Moreover, Cooper merely teaches testing the ECC generation function by writing into memory, with the ECC generation function being disabled, an ECC code and a test pattern that does not generate this ECC code,

and by reading the test pattern to perform an ECC check while the ECC generation function is enabled.

In contrast, the present invention provides that the information about the presence or the absence of an ECC error is output to the exterior of the semiconductor memory device in response to a predetermined command input after a data read operation. Neither Kishino nor Cooper teaches or suggests this feature. It is submitted that this distinguishing feature provides for an external system to obtain information about defective blocks by referring to the information about the presence or the absence or an ECC error after a data read operation. Therefore, the present invention provides an easy management of defective blocks.

Accordingly, Applicant submits that the cited prior art fails to disclose or suggest each and every element recited in claim 7 of the present application, and therefore is allowable.

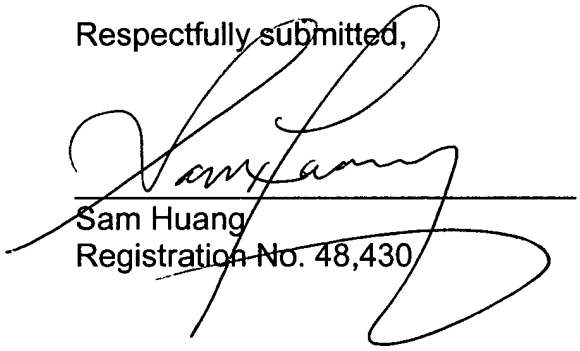
As claims 8 and 9 depend from claim 7, Applicant submits that each of these claims incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to the independent claim.

In view of the above, Applicant respectfully submits that each of claims 1-4 and 7-9 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-4 and 7-9 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 100353-00069.

Respectfully submitted,



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Enclosures: Petition for Extension of Time (1 month)